I. PRELAB FOR ALIASING LAB

You might expect that to record a frequency of 4000 Hz you would have to sample at a rate of at least 4000 Hz. It turns out, however, that you actually have to sample at TWICE that rate (the Nyquist theorem) This is because you need to record a peak and a valley from each cycle. If you sampled at the same rate that the signal was oscillating, you would get a peak every time you sampled, and the output would be a constant voltage.

When you sample at a rate that is less than twice the signal frequency, the output frequency is lower than it should be. This phenomenon, called “aliasing” or “foldover”, is best studied by trying it.

Fill in the following worksheet-style pages. A colored pen or pencil works best. The procedure is:

1. Start at the left edge of the paper; at this point the signal is at its maximum value.

2. Draw a straight line to the right for the number of squares indicated in the left hand margin.

3. Drop straight down until your pen is BELOW OR EQUAL TO the signal.

4. Go right again for the appropriate number of squares. Each time you get to sample, move your pen to the highest corner which is below or equal to the signal.

5. Continue.

ALWAYS STAY ON THE GRID. Never cut across squares. Trace the example to get a feel for it.

Notice how the quality of reproduction decreases as the sampling rate decreases. In the last examples on the first workpage (page 2) the sampling frequency is more than half the signal frequency. Observe the consequences. This is aliasing.

On the pages 3 and 4, the frequency of the signal stays the same, but we keep changing the sampling period. What is the apparent period (in divisions) of each signal after it is sampled?
II. ALIASING (FOLDOVER) LAB

A. Set Up

Your ADC and DAC should be intact from last lab. Attach the scope and function generator. Make sure that everything still works.

Set up the scope so that you can look at the original and final signals simultaneously. Put the final output of the DAC on CH2 so you can invert it. Set the generator to a 100 Hz sine signal and maximum amplitude without causing clipping at the output (recall that you need to use the DC offset on the generator so that the signal is always positive).

Set the MODE knob to CHOP and the INTernal TRIGger to CH1. Adjust the position knobs and the red UNCALibrate knob on CH2 so that the two signals exactly overlap.

Vary the frequency knob and watch the two signals move together.

B. Limits of Digitization

There are two characteristics of a digital system which limit it’s accuracy: number of bits and rate of sampling.

1. Number of Bits

You are using only four bits (16 possible voltages), yet the picture of the sine voltage after digitization is recognizable. Of course, the quality of the output deteriorates for smaller input signals because fewer bits are being used. Observe this by turning down the amplitude of the function generator. Adding bits is a good way to make the signal more accurate because each bit DOUBLES the overall accuracy. Increasing the number of bits from 4 to 16 would take 4 times as much memory, but would make the output 4096 times more detailed. With 4 bits, the dynamic range is \((20 \text{ dB}) \times \log(2^4) \approx 24 \text{ dB}\); CD’s use 16 bits (a theoretical dynamic range of 96 dB).

Set your function generator back to 100 Hz and maximum amplitude before proceeding.

2. Rate of Sampling

The number of bits determines the Dynamic Range of a digital system. The Frequency Range is determined by the sampling rate, or number of numbers recorded per second. Unfortunately, in order to double the frequency range you must also double the sampling rate. Furthermore, as you saw in your prelab, you have to sample at TWICE the rate of the highest frequency you want to record. For audio signals this means you need to record a 16 bit numbers more than 40,000 times EVERY SECOND per channel. That means a 60 minute stereo recording requires a minimum of 5 billion bits of storage.
Your ADC is currently hooked up to run at its fastest rate. Its effective sampling time is the amount of time it takes to make each conversion. Sampling rate problems are more easily observed with a slower rate. To do this connect a 100 pF capacitor from pin 4 (the clock input) to ground. Also, hook the output of your op amp to your headphones THROUGH A 2200 OHM RESISTOR. (This will probably require using a little breadboarding wire to take the signal to one of the banana plugs on the breadboard that is mounted to the table.) Vary the frequency as you listen to the digitized output. You should be able to hear the signal plus the high, whiny sampling noise. In a real reproduction system this would be filtered out. Switch to the 1 kHz range. Notice that as you increase the frequency the output signal starts to lag the input.

Switch to the 10 kHz range. SLOWLY increase the frequency with the triggering on CH1. At some point you will hear the output frequency will top out and start falling EVEN THOUGH YOU KEEP INCREASING THE FREQUENCY OF THE INPUT. This is called “aliasing.”

At what frequency $f_{\text{max}}$ does this occur?

What is the PHASE relationship between input and output at this frequency?

As you keep turning the frequency up, you come to a point where the output frequency drops to zero (the output is close to DC), and then starts increasing again. What frequency is this?

Keep turning the frequency up until the output tops out and folds over again. How high is this compared to the $f_{\text{max}}$?
It is easier to see what’s going on the digitized output if you look only at CH2 and trigger on CH2. Slowly increase the input frequency and watch the output frequency go up and down. Ask your instructor if you need assistance with this.

Calculate the sampling time. To do this, set the frequency just above \( f_{\text{max}} \). The output will look something like this:

![Sampling Time Diagram](image)

Use the scope to measure the sampling time (the time interval from the beginning of one transition to the beginning of the next):

Calculate the sampling frequency = \( 1/(\text{sampling time}) \).

Compare this with the frequency \( f_{\text{max}} \).
Now remove the 100 pF capacitor, thus increasing the clock rate.

Measure the new sampling time.

Calculate the new sampling rate.

Predict the new $f_{\text{max}}$.

Now measure $f_{\text{max}}$ directly by listening to the DAC output.
3. **Problems with digital sound reproduction**

We have now heard two key problems with digital sound reproduction: sampling whine and aliasing. These can both be addressed by using filters.

**a. Output Filtering**

Reinsert the 100 pF capacitor between pin 4 (the clock input) of the ADC to ground. Place a 0.1 µF capacitor (call this value CF) between pins 6 and 2 of your DAC (this will effectively filter the DAC output by rolling off the gain of the inverting amplifier by 6dB/octave for frequencies above \( f_c = \frac{1}{2\pi RF CF} = \frac{1}{2\pi \times 2.5 \times 0.1 \mu F} \approx 640 \text{ Hz} \).  

Listen to the output using the headphones. Most of the sampling noise should be gone. Look at the smoothed output on the scope. What happens as you increase the frequency to approach \( f_{\text{max}} \)? What happens for input frequencies above \( f_{\text{max}} \)?

Problems remain even with output filtering: 1) it does not remove the effects of aliasing and 2) it distorts the output for frequencies between \( f_c \) and \( f_{\text{max}} \), where we probably want a flat response. We can fix problem 2 with a better filter, but problem 1 requires input filtering (before the ADC).
b. Input filtering

The only way to reduce the effects of foldover is to filter the signals going into the input of the ADC. What considerations should go into the design of this filter? We do not want to distort the input signal for frequencies below f_{max} and we want a very fast rolloff above f_{max}. This calls for a high-order low pass filter.

We can verify that an input filter will improve aliasing by putting the signal through a second-order low pass filter before the input of the ADC. This filter has it's cutoff frequency (-3 dB point) at 4 kHz and rolls off approximately -12 dB at 8 kHz. The low frequency gain is close to unity because of the voltage divider at the output.

![Filter Circuit Diagram]

Try it out: Is there a noticeable reduction in aliasing?